# Tracking Detectors 2 – silicon for HEP

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# Acknowledgements

- Many of the slides shown here come from a presentation generously lent to me by Dr Cinzia Da Via (Manchester). Her slides are individually identified in this talk.
- One slide was kindly lent to me by Professor Geoff Hall of Imperial College.
- Some come from collaboration WWW sites

# Resources (Books)

- Silicon Solid State Devices and Radiation Detection, Leroy & Rancoita, 2012
- Pixel Detectors, Rossi, Fisher, Rohe & Wermes, 2006
- Semiconductor Detector Systems, Spieler, 2005
- Semiconductor Radiation Detectors, Lutz, 1999

# Resources (Conferences)

See the proceedings (recent ones on Indico) of the **Vertex 20XX** and the **Pixel 20XX** conferences for example.

Vertex 2016: https://indico.cern.ch/event/452781/overview
Pixel 2016:
https://agenda.infn.it/conferenceDisplay.py?ovw=True&confId=10190

# What is a silicon detector?

- It is a member of a large family of *ionisation* detectors.
- Related to the gaseous or liquid argon detectors but based on a solid material.
- Nearly all silicon detectors are based on a junction diode. The diodes are reversed biassed until fully depleted.
- A MIP particle passing through silicon creates about 8000 electron/hole pairs per 0.1mm. A typical detector element is about 0.3 mm thick.

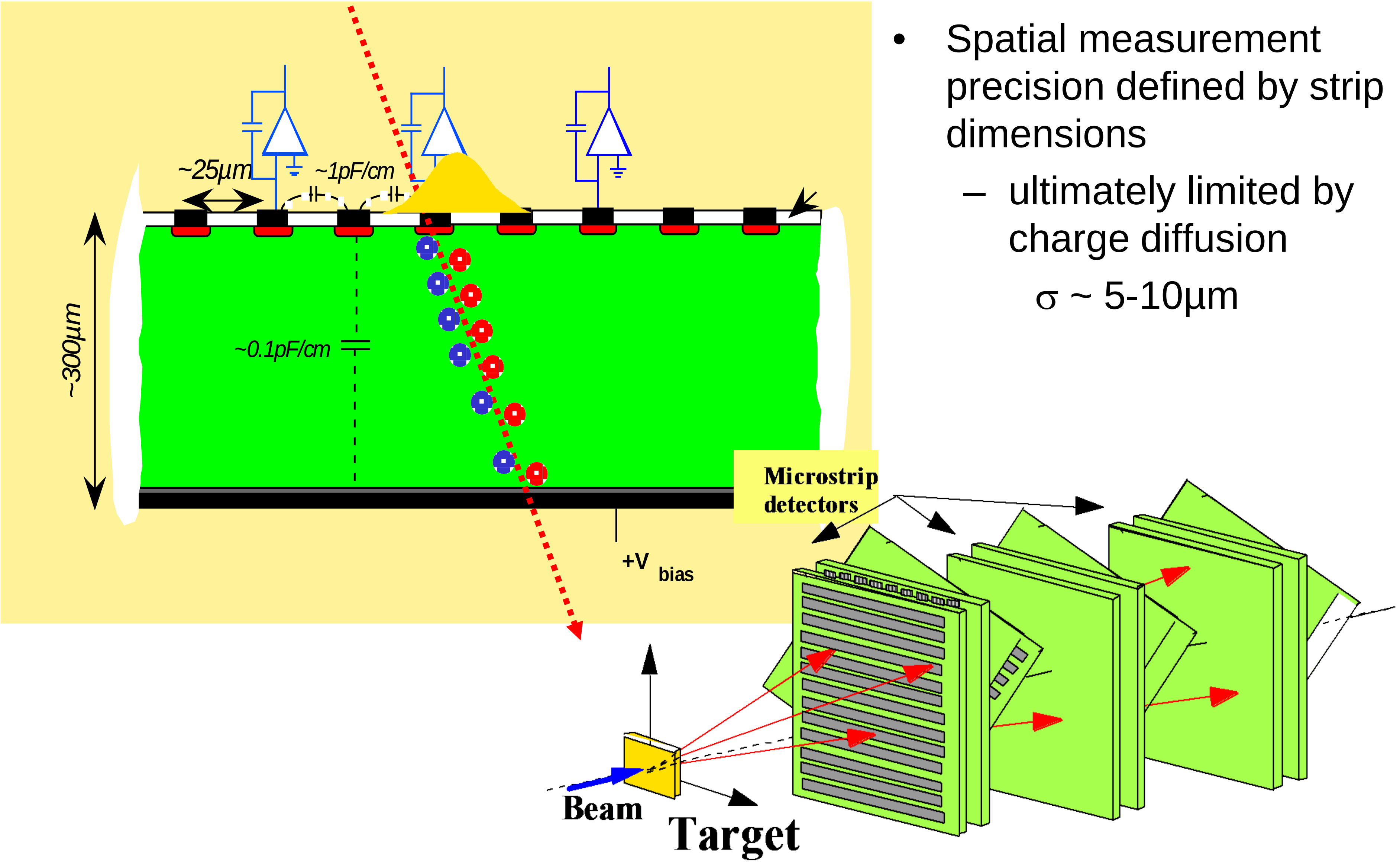
# Basic types

- Silicon strips
  - Implanted p on n gives a single sided detector
  - Adding an $n^+$ implant on the other side makes a double sided detector
  - Typical strips have a pitch of order 0.1 mm
- Pads
  - On single sided detectors. Pads are typically $0.1 \times 0.1$ mm$^2$
- Pixels
  - Smaller than pads. The CCD is a special (and important) example of a pixel detector e.g. SLD vertex detector at SLAC.

# Silicon diodes as position detectors

- Spatial measurement precision defined by strip dimensions
  - ultimately limited by charge diffusion

    σ ~ 5-10µm



# Examples

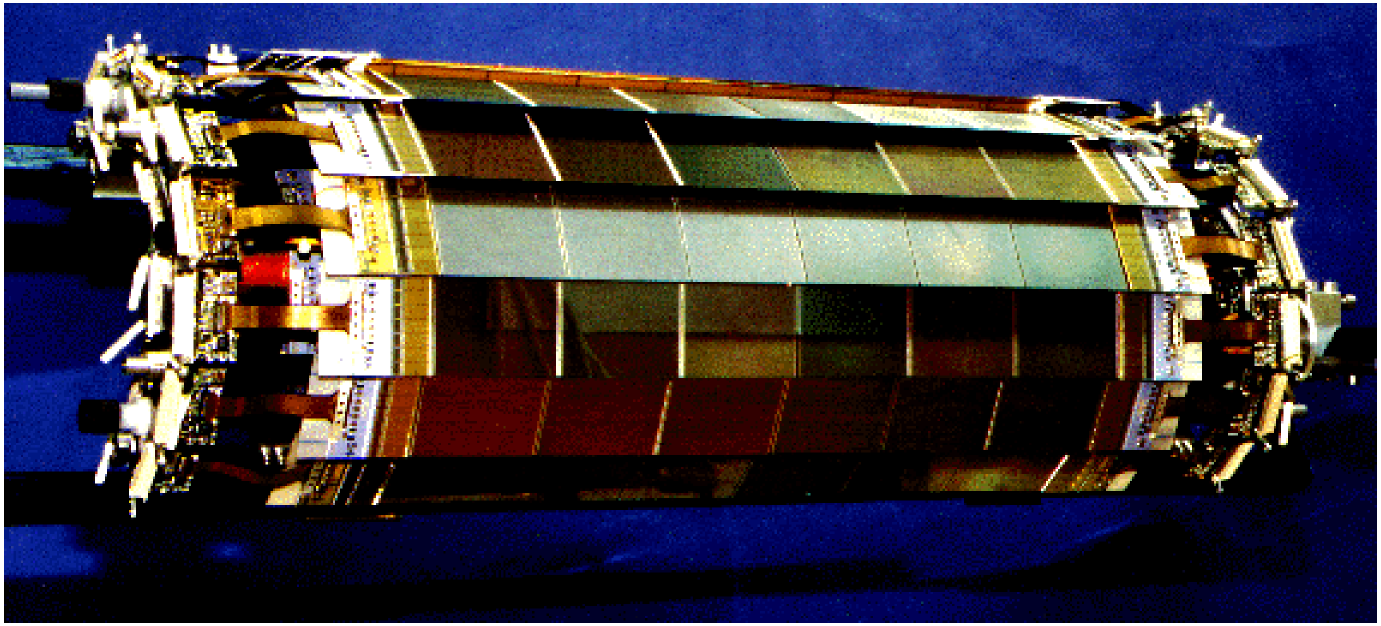
- In 1983 NA11 pioneered the use of silicon for track reconstruction in a fixed target experiment to measure charmed particle lifetimes. A readout pitch of 60µm (3 times the actual pitch) was used and a spatial resolution of 5 µm achieved.
- At this time CCD detectors were also being developed for tracking detectors

# Examples - LEP

- “Complete” $4\pi$ coverage of silicon detectors for tracking at colliders was a feature of LEP experiements in the 1990’s.
- Major challenge is to package the readout electronics
- ALEPH was first to use double sided vertex detector.
  - Two cylinders with a total of 27 faces each with 4 detectors of 50x50 $mm^2$.
  - Readout at 50 µm in $r$-$\phi$ and 100 µm in *z.*
  - *Multiple scattering* reduced the intrinsic resolution of 12 µm  and 17 µm to 20 µm  and 40 µm.
- All 4 LEP experiments upgraded to silicon vertex detectors during their operational lifetime.

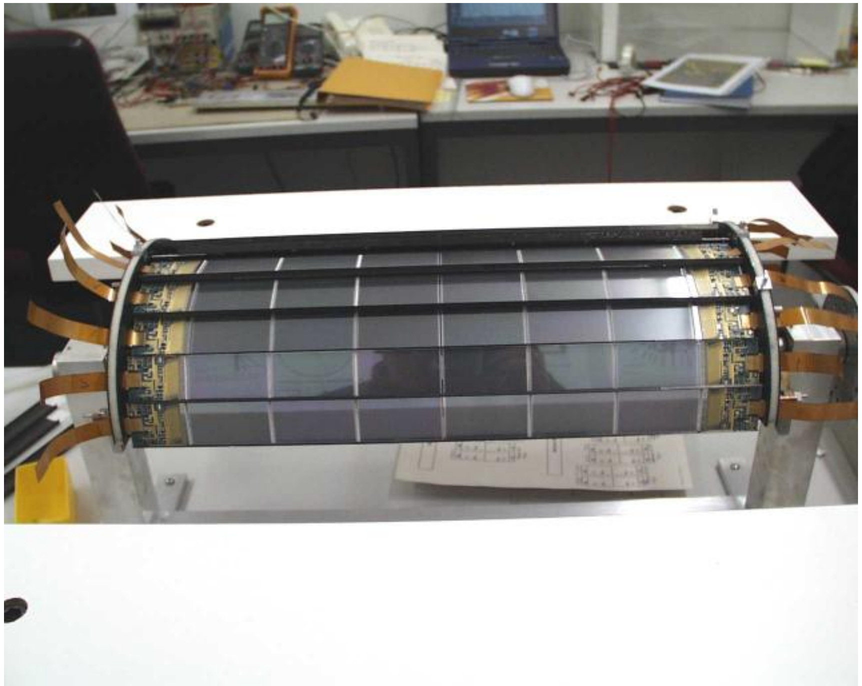
# Aleph

- The silicon vertex detector, 1995 version

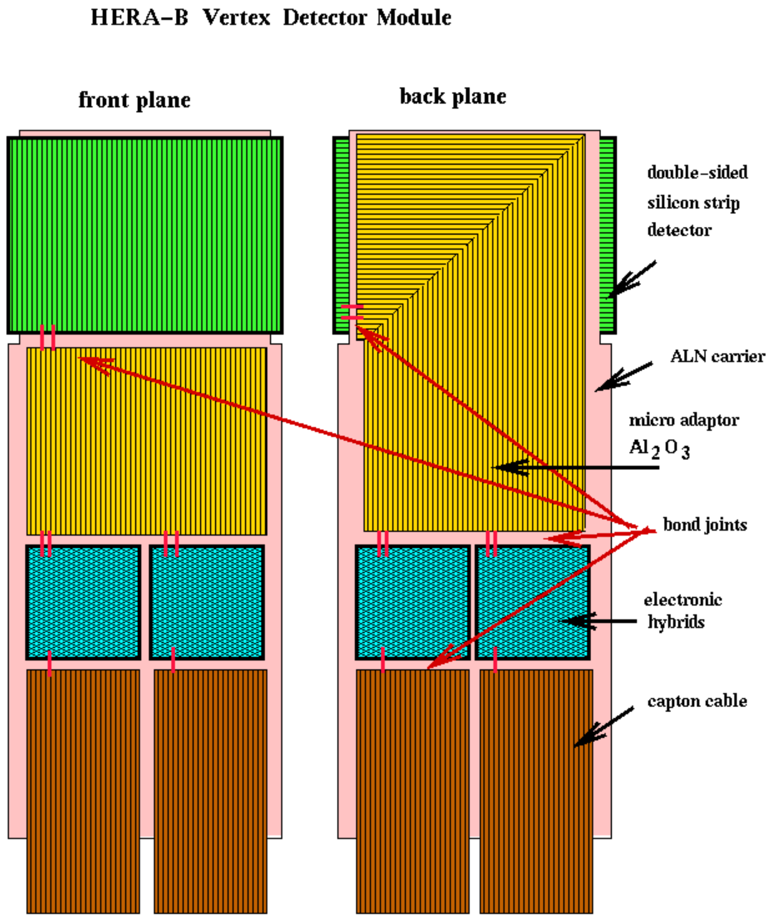


Aleph WWW site publicity picture

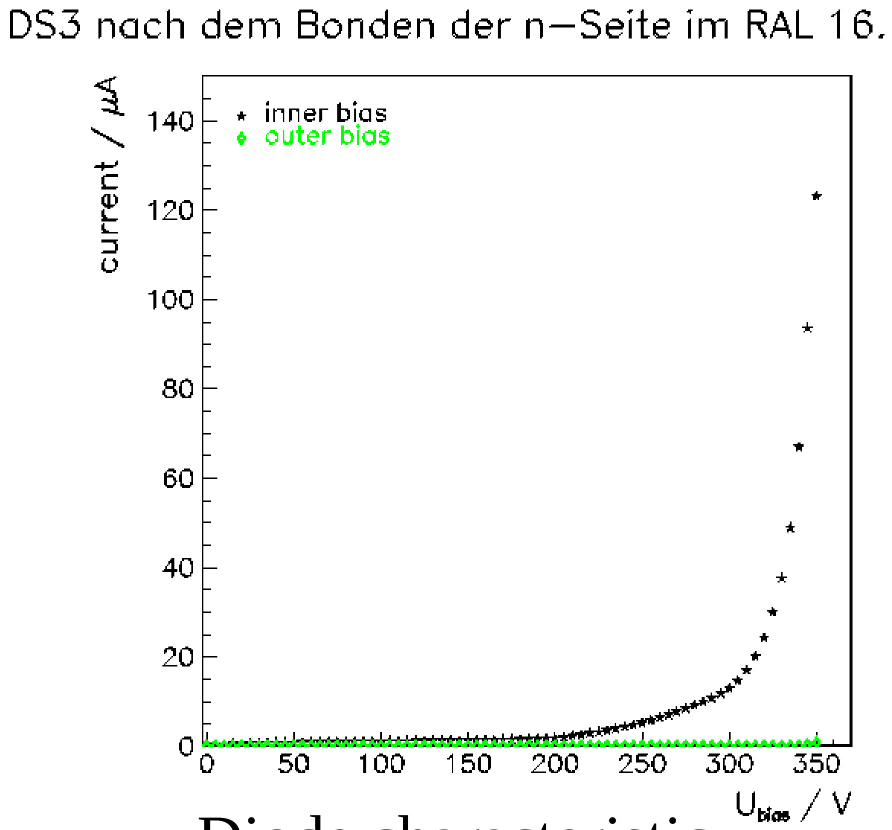
# H1 at DESY



# HERA B



Hera B figures

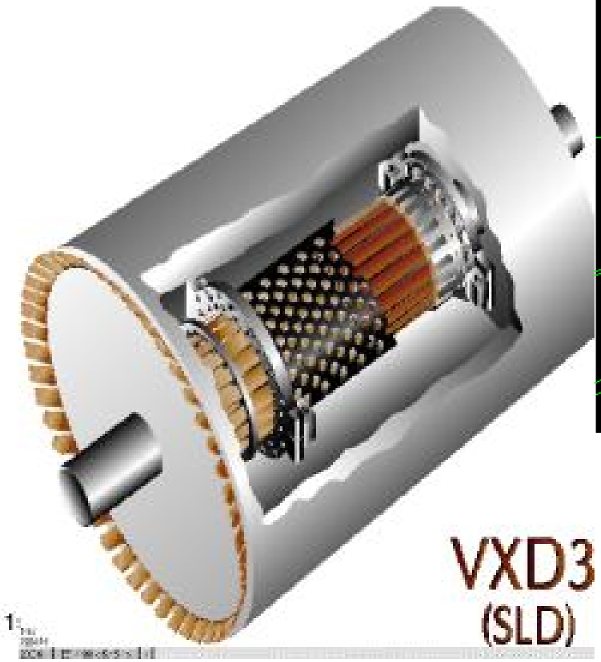


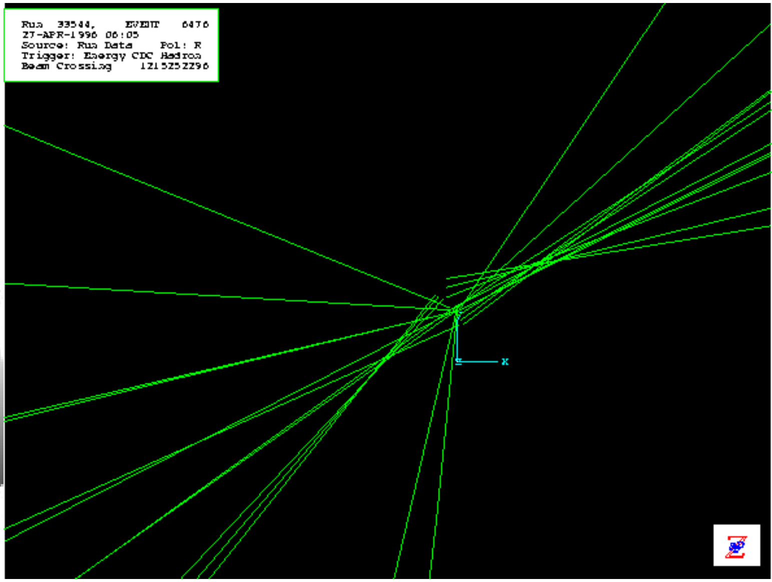
Diode characteristic

# SLD

## CCD - VXD3 at SLAC

- Very thin, 0.4% radiation length
- High resolution
  - pixels - 20 µm cubes
  - surface resolution < 4 µm
  - projected impact parameter resolution 11 µm
- Close to beam, inner layer at 2.8 cm radius
- 307 million pixels, < 1 cent/pixel



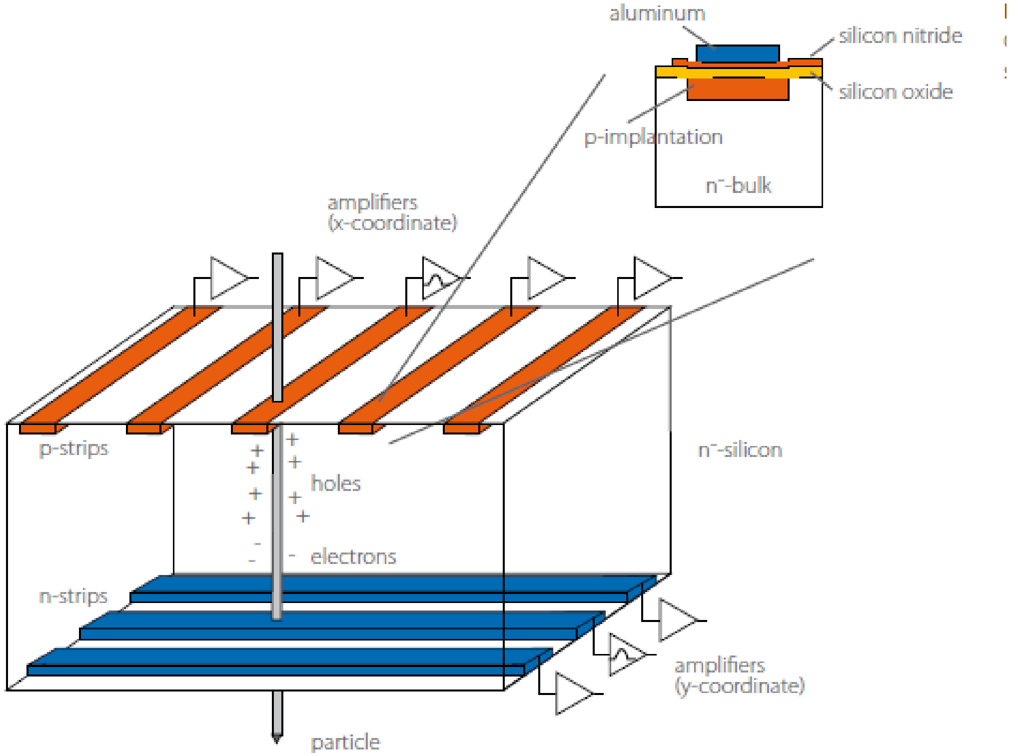


```
Run  33544,     EVENT   6476
27-APR-1996 06:05
Source: Run Data     Pol: R
Trigger: Energy CDC Hadron
Beam Crossing    1215252296
```

bb event from
SLD WWW site

Figure from talk by H Wieman at Vertex 2000

# Double-sided strip



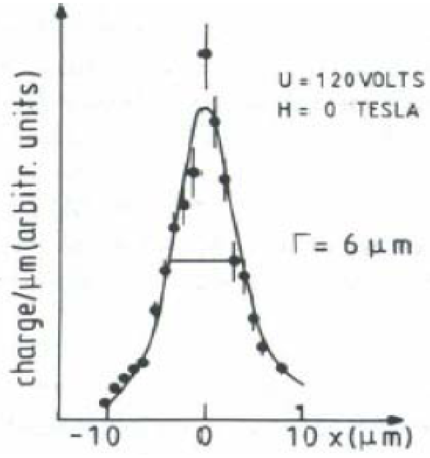
Principle of the double-sided strip detector.

Picture from MPI-HLL (2007)

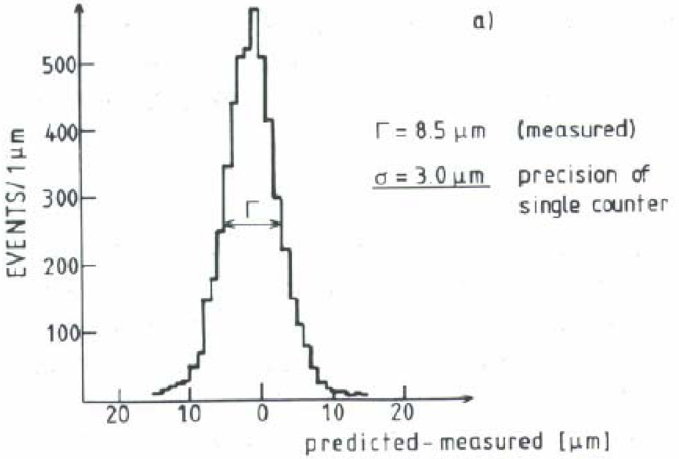
# Resolution

spatial resolution: strip pitch with interpolation by diffusion (~10 μm)

measured distribution of holes at $p^+$ strips

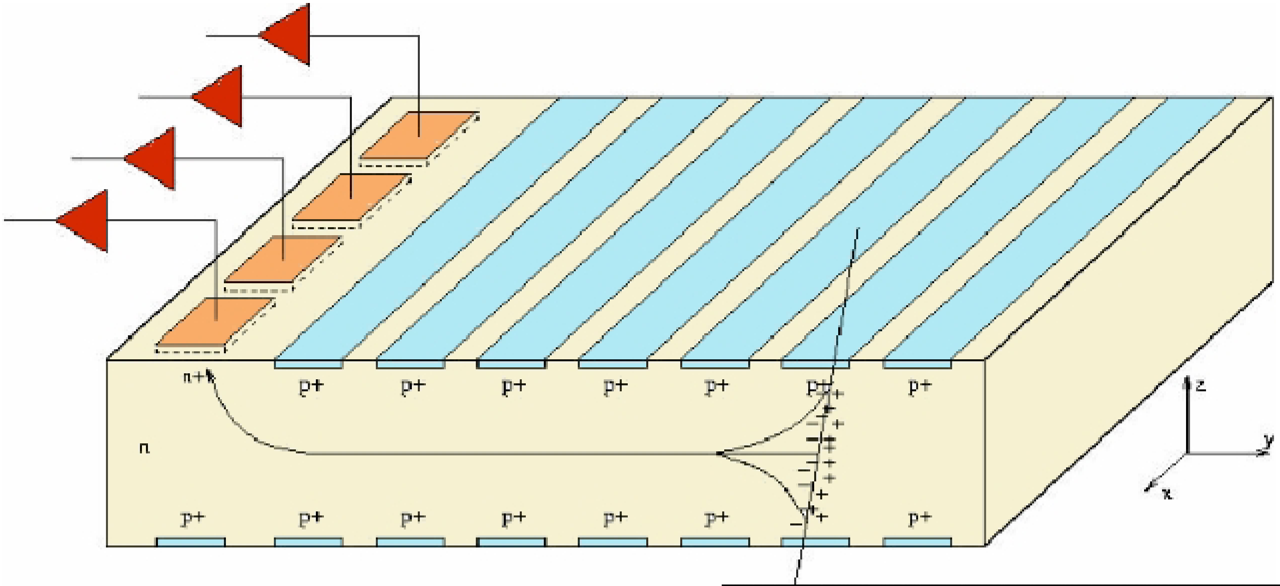


achieved resolution: ~ 1μm (detector with 20μm pitch NIM235(1985)210)

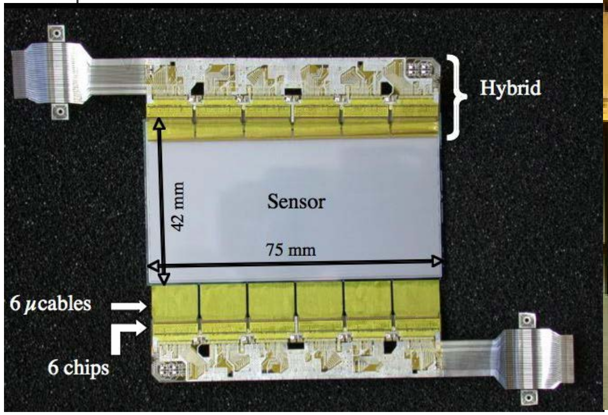


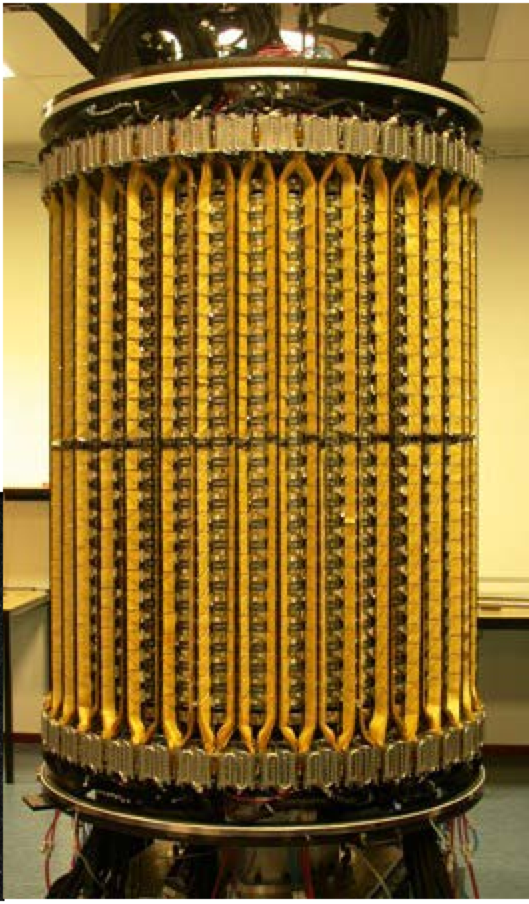
From a lecture by Robert Klanner, Univ. Hamburg

# Silicon Drift Detector



The Inner Tracking System of the ALICE experiment at LHC uses Silicon Drift Detectors in two cylindrical layers located at radial distance of ≈ 15 and ≈ 24 cm from the beam axis.



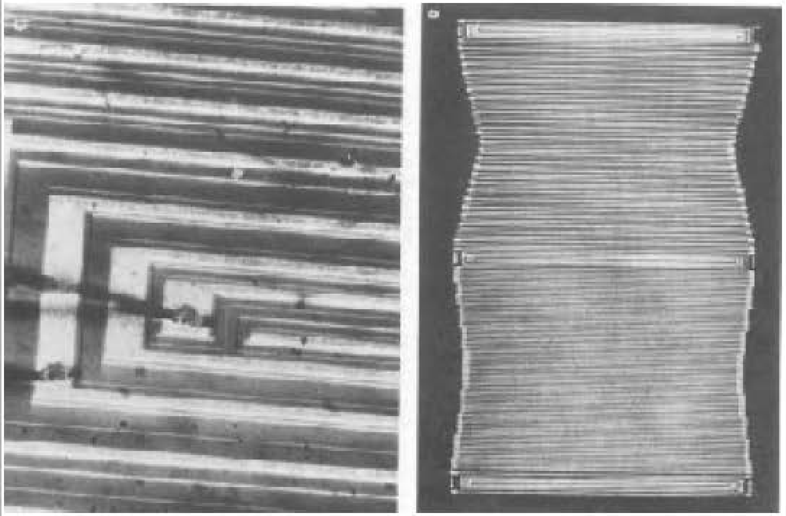


SDD for ALICE

Pictures taken from G.Contin “The Silicon Strip Detector (SSD) for the ALICE experiment at LHC: construction, characterization and charged particles multiplicity studies.” PhD thesis, Trieste, 2008

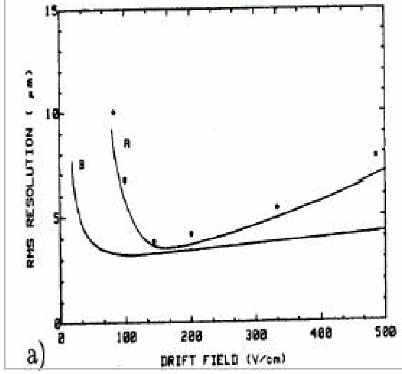
# Silicon Drift - examples

- first realisation (NIM235(1985)231)

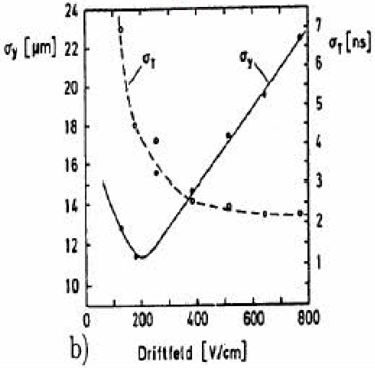


- position resolution vs drift field →
  ~ 5μm achieved

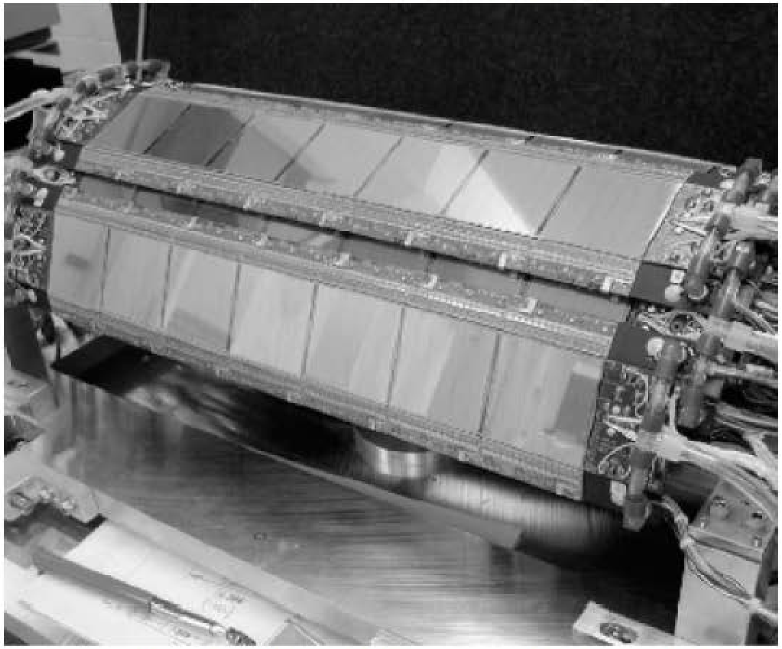
Laser spot



beam particles



example of a vertex detector based on Si-drift chambers (STAR detector at RHIC, BNL - NIMA 541(2005)57)

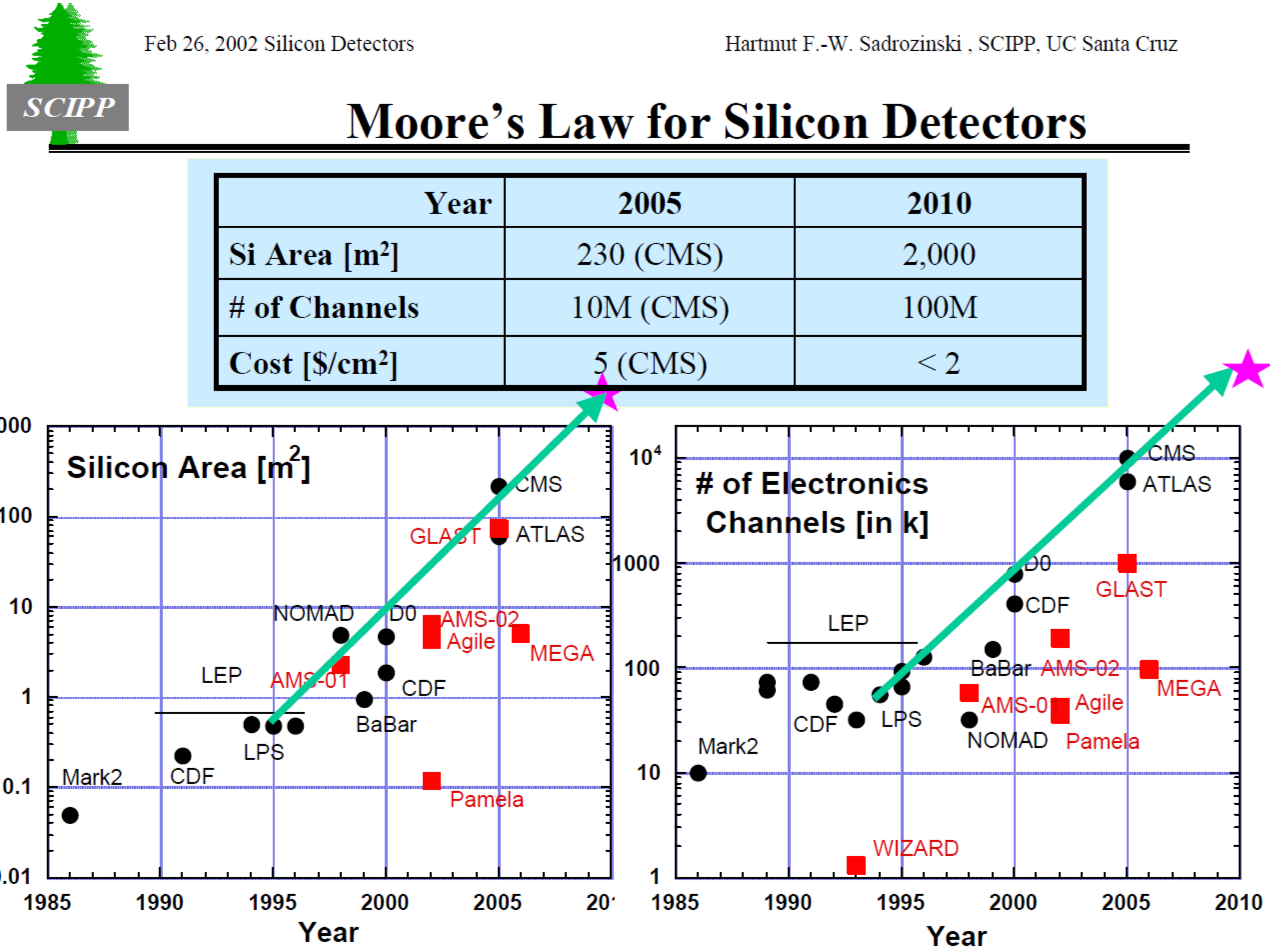


- excellent 2d position resolution with small no. of read-out channels but
- speed (several 100 ns drift times)
- sensitivity to radiation

drift principle → many applications!

From a lecture by Robert Klanner, Univ. Hamburg

# Evolution of scale



SCIPP

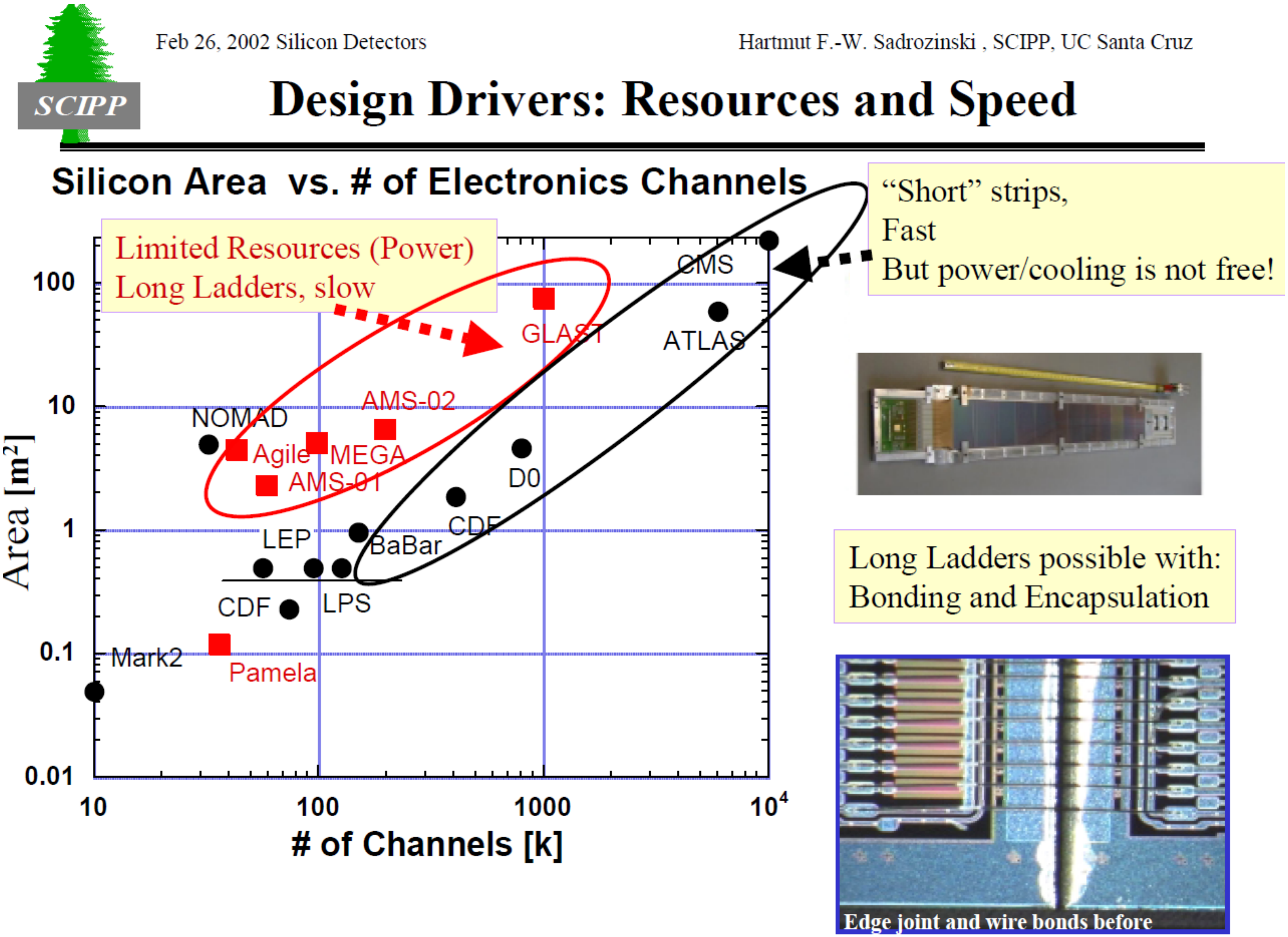
Feb 26, 2002 Silicon Detectors

Hartmut F.-W. Sadrozinski , SCIPP, UC Santa Cruz

## Moore’s Law for Silicon Detectors

| Year | 2005 | 2010 |
|---|---|---|
| Si Area [m²] | 230 (CMS) | 2,000 |
| # of Channels | 10M (CMS) | 100M |
| Cost [$/cm²] | 5 (CMS) | < 2 |

# Growth with time



Feb 26, 2002 Silicon Detectors

Hartmut F.-W. Sadrozinski , SCIPP, UC Santa Cruz

SCIPP

## Design Drivers: Resources and Speed

**Silicon Area vs. # of Electronics Channels**

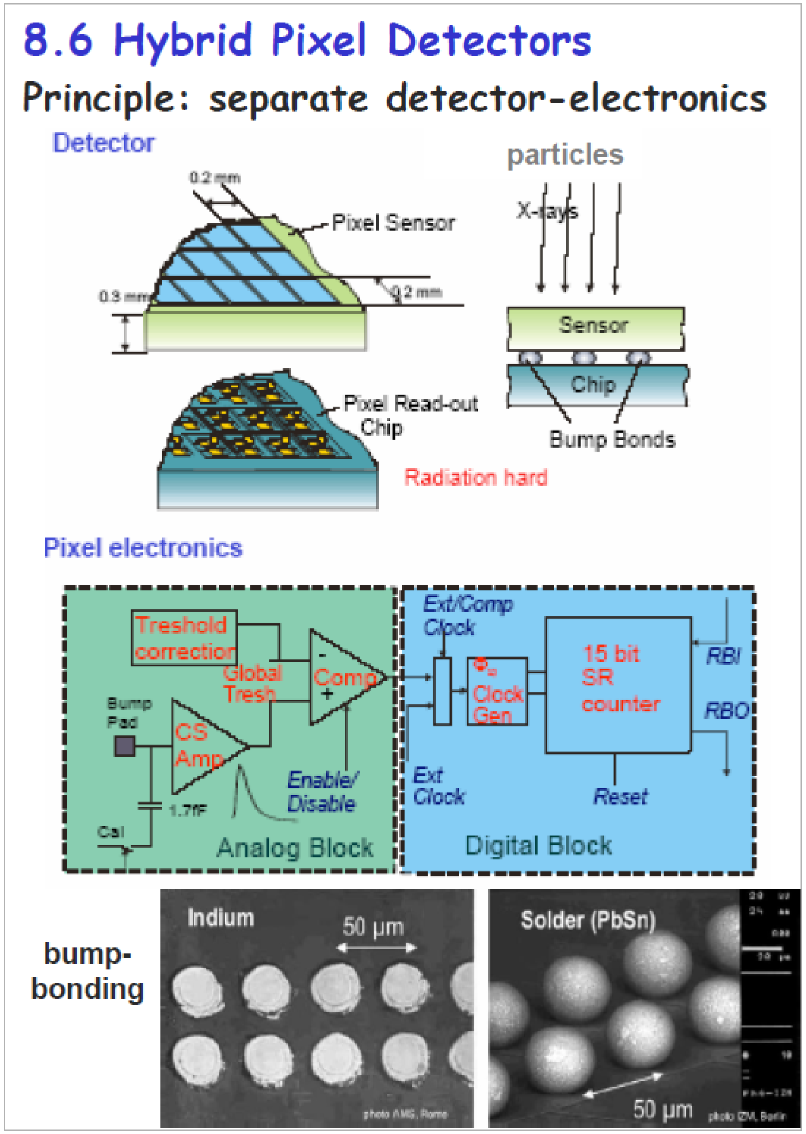
Limited Resources (Power)
Long Ladders, slow

"Short" strips,
Fast
But power/cooling is not free!

Long Ladders possible with:
Bonding and Encapsulation

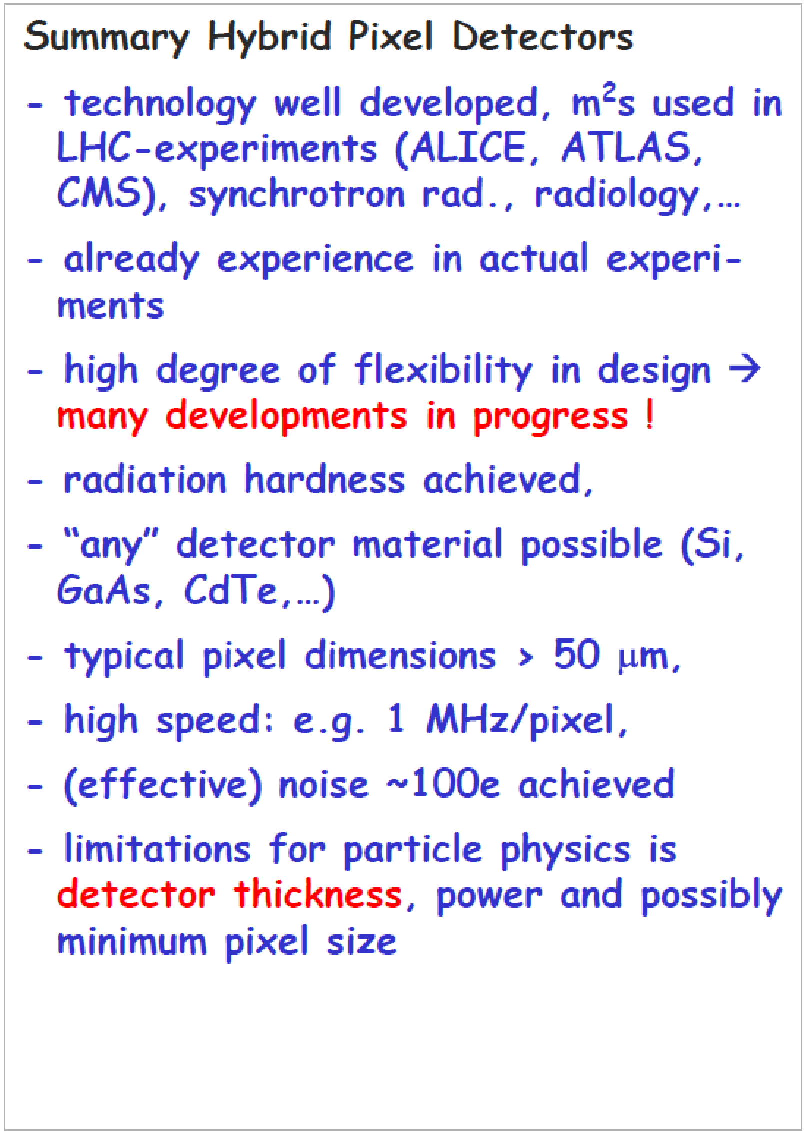
Edge joint and wire bonds before

# “Hybrid” Pixels



## 8.6 Hybrid Pixel Detectors

Principle: separate detector-electronics



## Summary Hybrid Pixel Detectors

- technology well developed, m$^2$s used in LHC-experiments (ALICE, ATLAS, CMS), synchrotron rad., radiology,…
- already experience in actual experiments
- high degree of flexibility in design → many developments in progress !
- radiation hardness achieved,
- “any” detector material possible (Si, GaAs, CdTe,…)
- typical pixel dimensions > 50 µm,
- high speed: e.g. 1 MHz/pixel,
- (effective) noise ~100e achieved
- limitations for particle physics is detector thickness, power and possibly minimum pixel size

From a lecture by Robert Klanner, Univ. Hamburg

# “Monolithic” Pixels

## 8.7 Monolithic Pixel Detectors

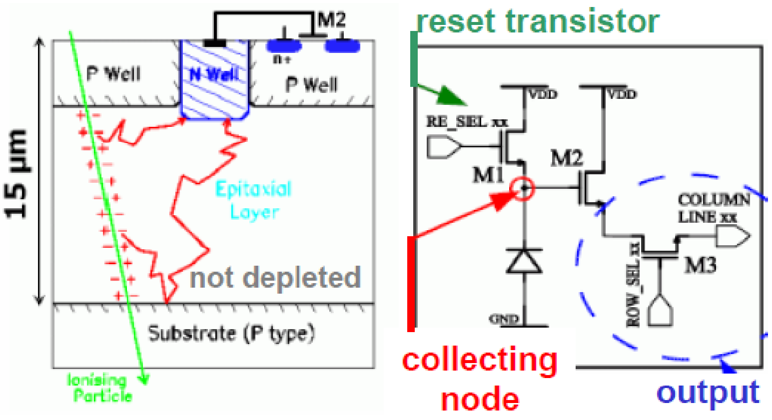
**Idea:** radiation detector + amplifying + logic circuitry on single Si-wafer

- dream! 1st realisation already in 1992
- strong push from ILC → minimum thickness, size of pixels and power !
- so far no large scale application in research (yet)

### CMOS Active Pixels

(used in commercial CMOS cameras)

**Principle:**

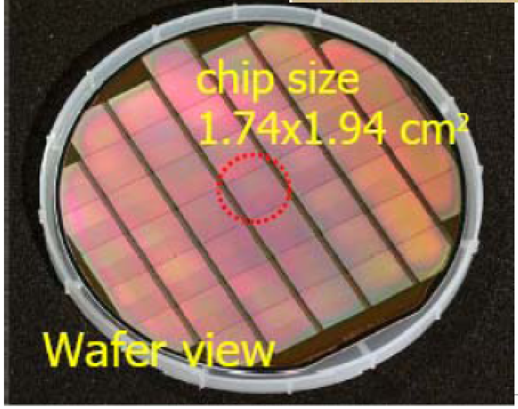


- technology in development – with many interesting results already achieved

**example:** MIMOSA (built by IReS-Strasbourg; tests at DESY + UNIHH)

3.5 cm² produced by AMS (0.6µm)
14 µm epi-layer, (17µm)² pixels
4 matrices of 512² pixels
10 MHz read-out (→ 50µs)
120 µm thick


Chip mounted on PCB board



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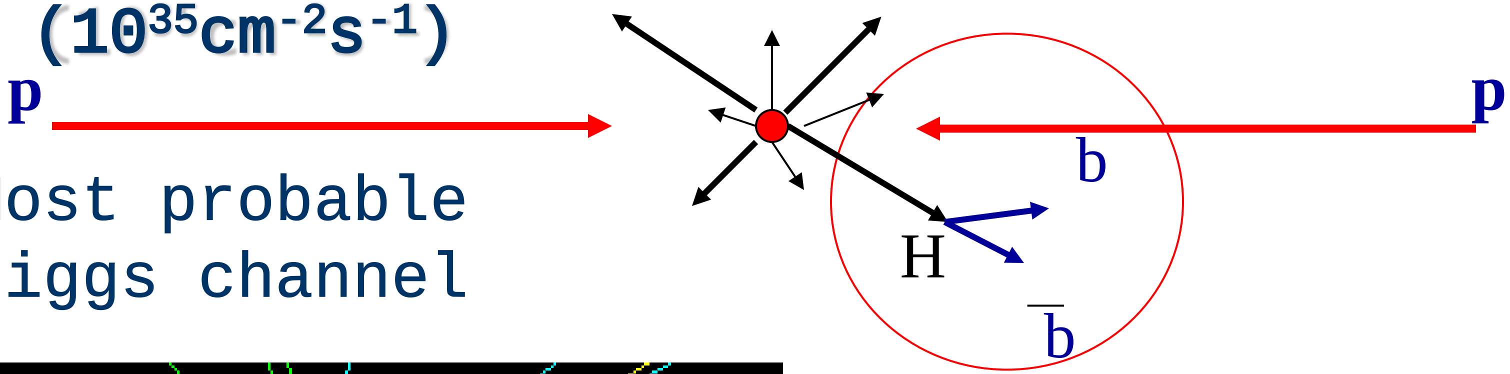
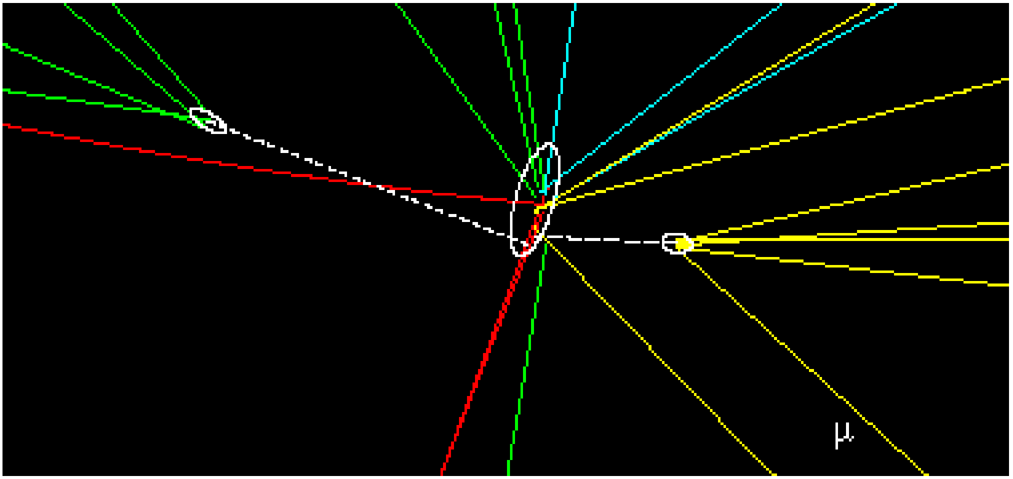
# PHYSICS REQUIREMENTS at the LHC and SLHC ($10^{35}cm^{-2}s^{-1}$)



Most probable Higgs channel



Aleph

**GOOD TRACKER ESSENTIAL!**

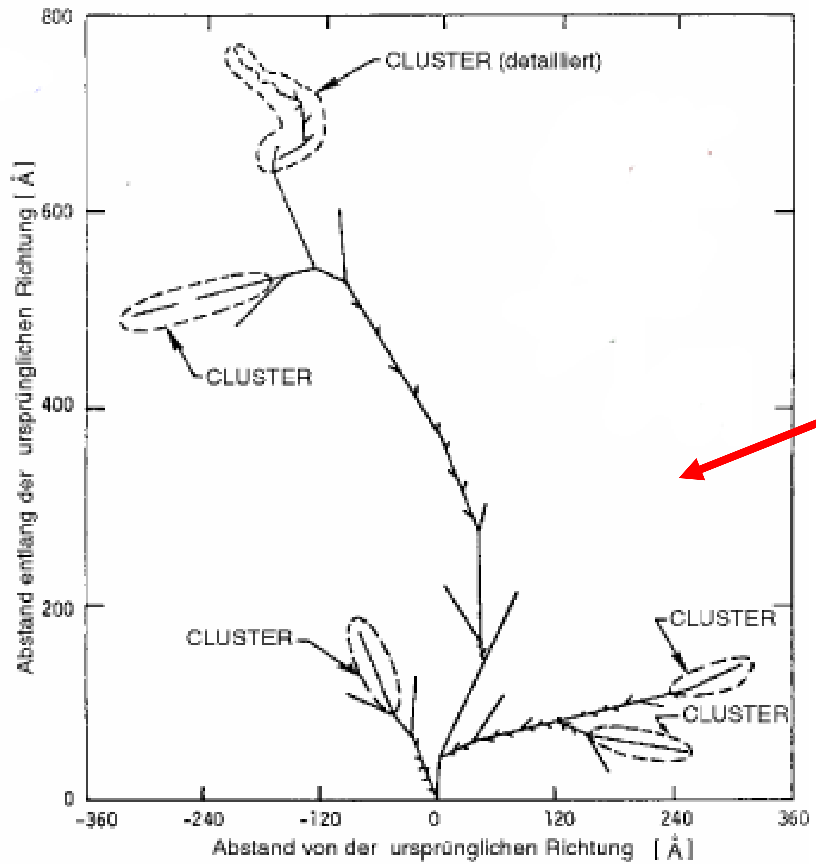
REQUIRED PRECISE MEASUREMENTS OF

- MOMENTUM RESOLUTION
- TRACK RECONSTRUCTION
- b-TAGGING EFFICIENCY

**HIGHER STATISTICS NEEDED FOR**

- ACCURACY OF STANDARD MODEL PARAMETERS
- ACCURACY OF NEW PHYSICS PARAMETERS
- SUPERSYMMETRIC PARTICLES
- EXTRA DIMENSIONS
- RARE PROCESSES (TOP DECAYS, HIGGS PAIRS ETC)

# RADIATION INDUCED BULK DAMAGE IN SILICON



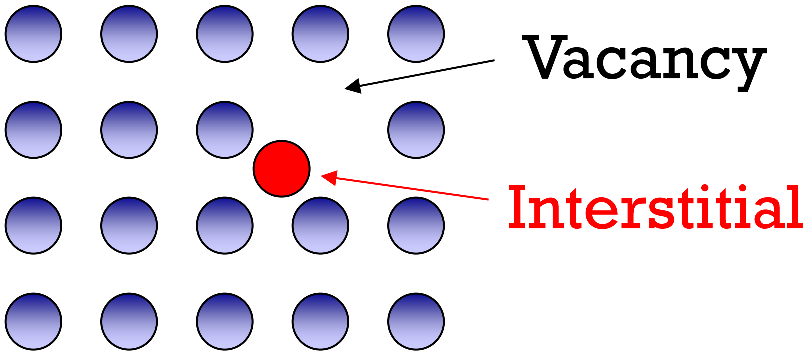
*Van Lint 1980*

Primary Knock on Atom

Displacement threshold in Si:

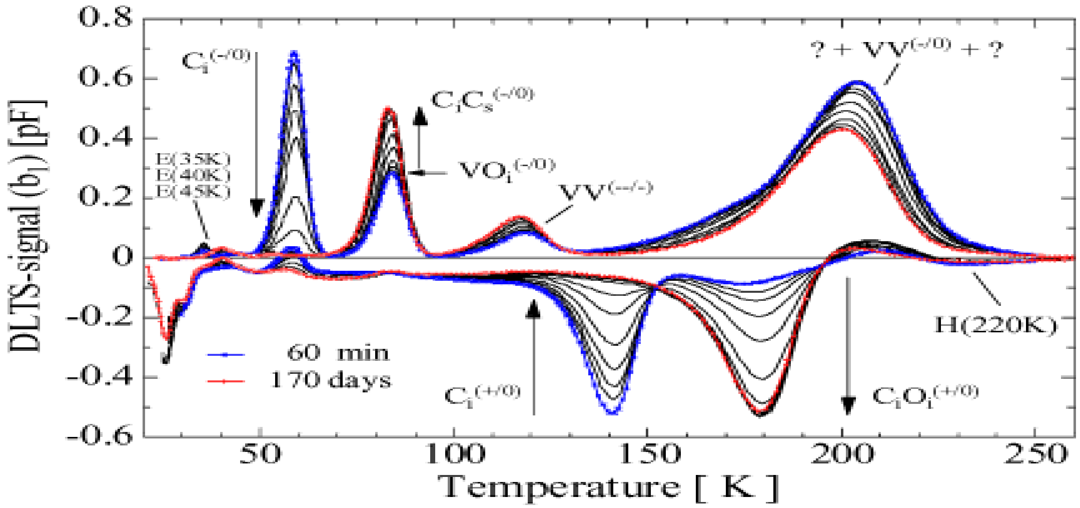
Frenkel pair E~25eV

Defect cluster E~5keV



# RADIATION INDUCED DEFECTS IN SILICON

**Neutron irradiated** *From RD48/rose* DLTS spectrum

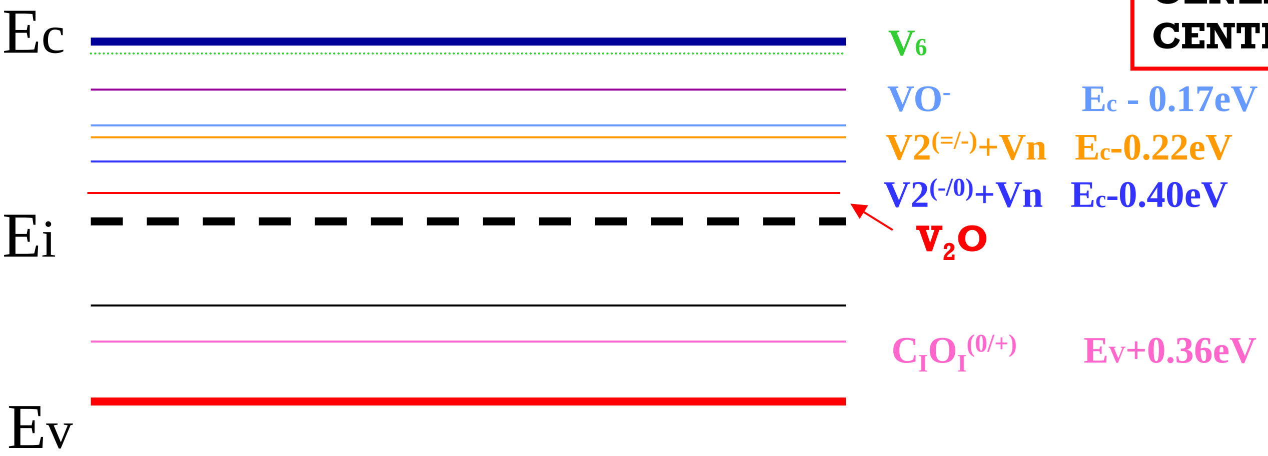


V,I MIGRATE UNTIL THEY MEET IMPURITIES AND DOPANTS TO FORM STABLE DEFECTS

**CHARGED DEFECTS**
**==>$N_{EFF}$, $V_{BIAS}$**

**DEEP TRAPS, RECOMBINATION CENTERS ==>CHARGE LOSS**

**GENERATION CENTERS==>LEAKAGE CURRENT**



$V_6$

$VO^-$ $E_c$ - 0.17eV

$V2^{(=/-)}$+Vn $E_c$-0.22eV

$V2^{(-/0)}$+Vn $E_c$-0.40eV

$V_2O$

$C_IO_I^{(0/+)}$ $E_v$+0.36eV

VO effective e and h trap

$V_2$ and $V_2O$ deep acceptors contribute to $N_{eff}$

# MAIN DETECTOR STRATEGIES AVAILABLE FOR LIFE ABOVE $10^{15}$ n/cm$^2$

## OPTIMIZATION OF:

- COLLECTION DISTANCE
- CCE (trapping)

- SPEED

- SPACE CHARGE
- REVERSE ANNEALLING
- CCE (underdepletion)

- CHARGE SHARING

- LEAKAGE CURRENT

## BY IMPROVING:

- DEVICE GEOMETRY
  3D, THIN

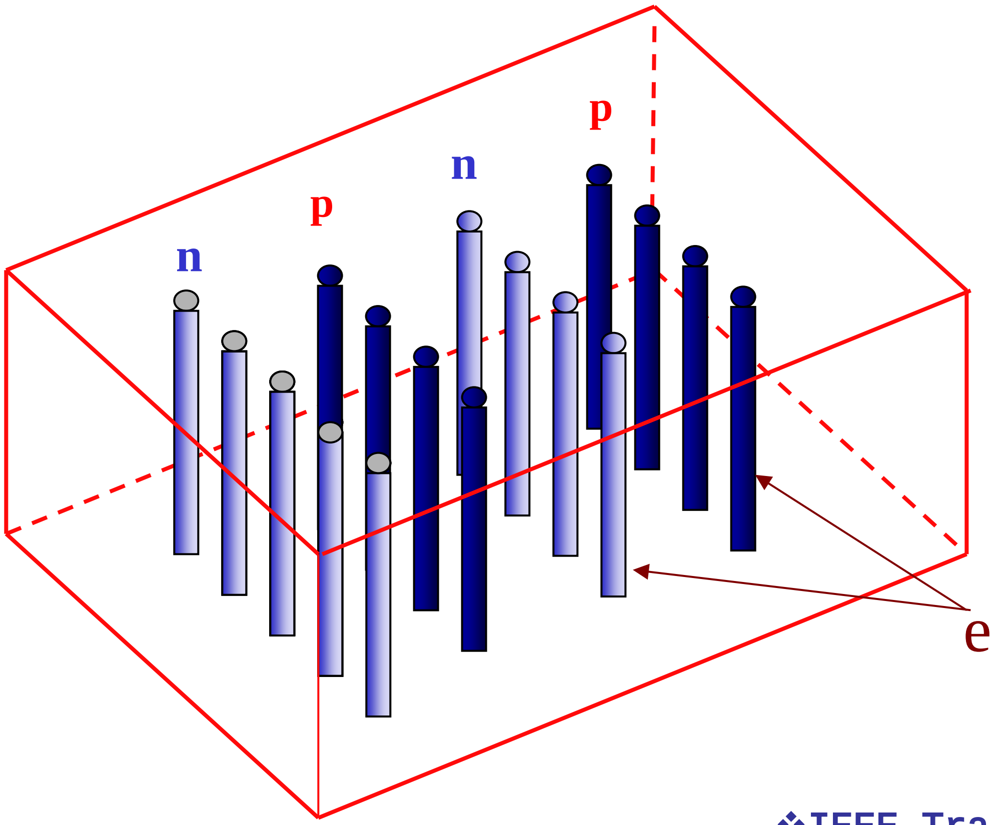
- DETECTOR BULK
  O, $O_2$ P-TYPE

- MODE OF OPERATION
  Temperature,
  Forward bias

**MORE TO GAIN BY COMBINING TECHNIQUES!**

# SHORT DRIFT LENGTH USING 3D DETECTORS

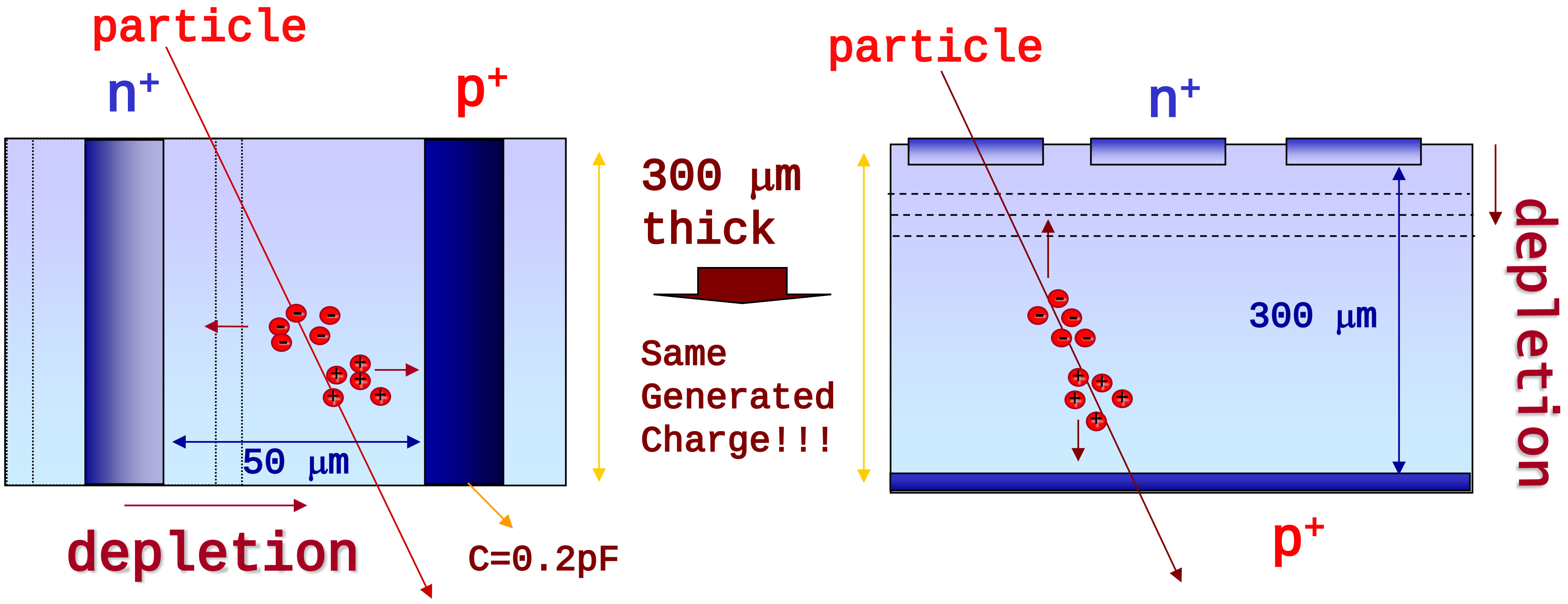
***S. Parker, C. Kenney***
***1995***



- ❖FZ silicon
- ❖p-type substrate
- ❖High resistivity kΩ–cm
- ❖<100> orientation

❖IEEE Trans Nucl Scie 46 4 (1999) 1224
❖IEEE Trans Nucl Scie 48 2 (2001) 189
❖IEEE Trans Nucl Scie 48 6 (2001) 2405
❖IEEE Trans Nucl Scie 48 5 (2001) 1629

# 3D VERSUS PLANAR



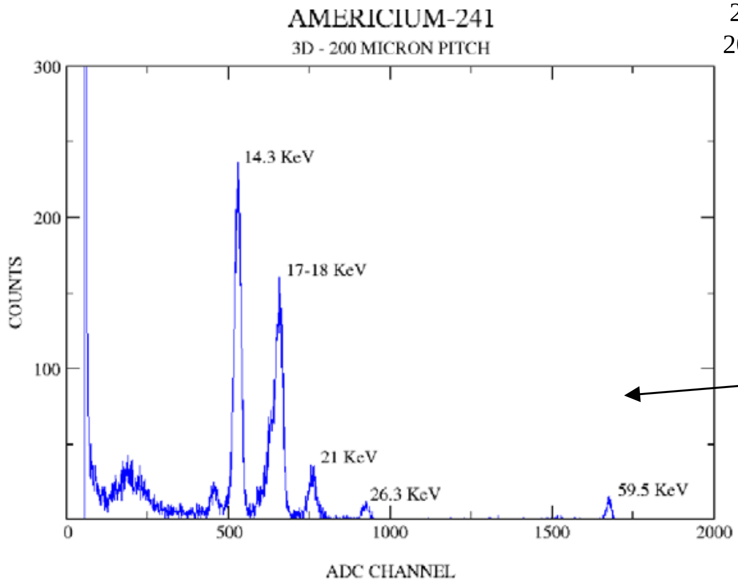
300 µm thick

Same Generated Charge!!!

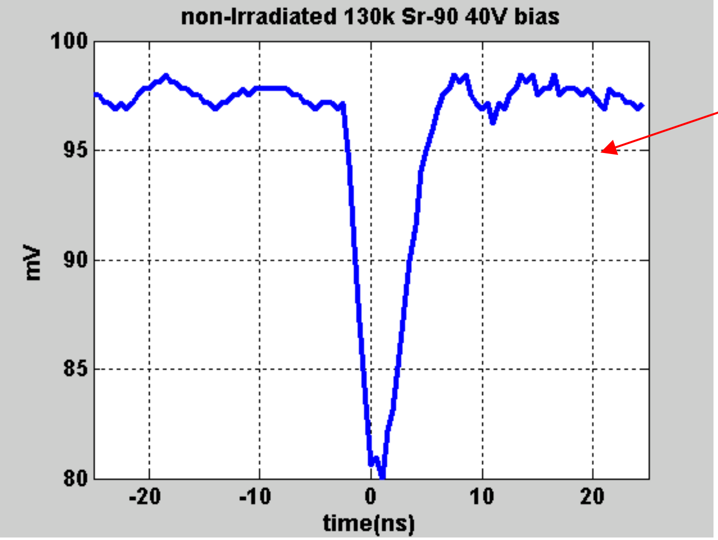
| | 3D | planar |
|---|---|---|
| ❖COLLECTION PATHS | ~50 µm | 300 µm |
| ❖DEPLETION VOLTAGES | < 10 V | 70 V |
| ❖CHARGE COLLECTION | 1-2 ns | 10-20 ns |
| ❖EDGE SENSITIVITY | < 10 µm | 300 µm |
| ❖AREA COVERAGE | active edges | other |

# 3D DETECTOR RESULTS before irradiation

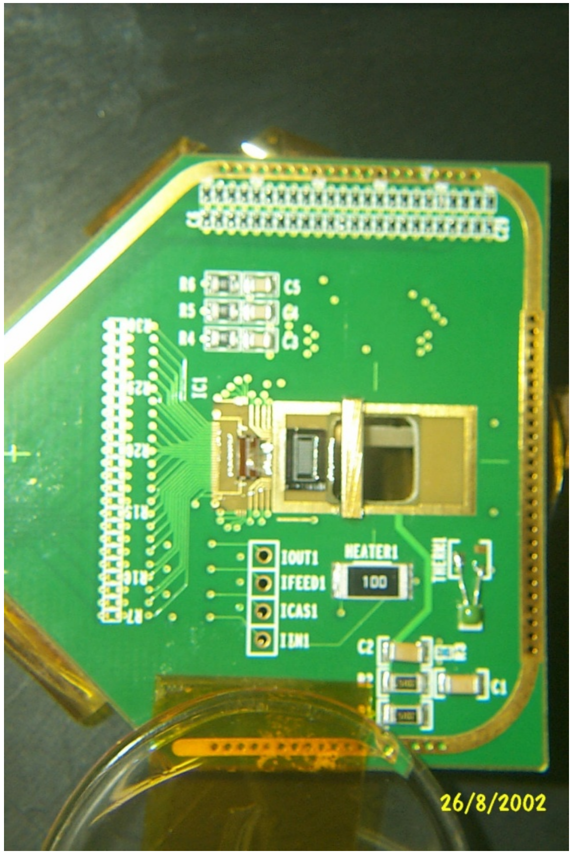
DETECTOR THICKNESS 121μm
282e noise PREAMP - SHAPING TIME 1 μs
200 μm PITCH μSTRIP TYPE DETECTOR



**GAUSSIAN RESPONSE**

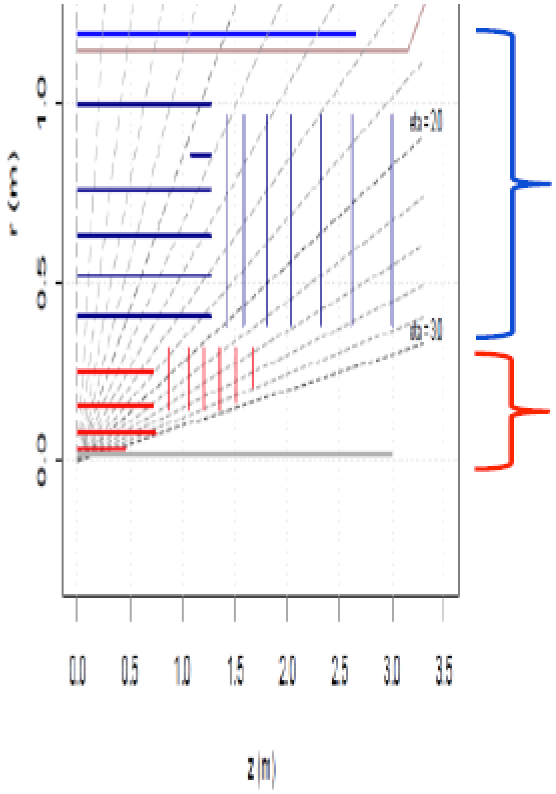


**SPEED**
**1.5ns rise**
**AT 130K**
**3.5ns rise**
**AT 300K**



350 e rms , fast electronic designed at CERN-microelectronics group
200μm pitch detector , Berunel, Cern, Hawaii, TO BE PUBLISHED

# Upgrades are in progress or planned for the LHC experiments



**Outer Trackers – Strips and strixels**

Bulk material type: p-type for higher signal and robust, cost effective process

Choice of FZ/MCz, thickness and oxygen concentration

Optimise strip geometry, length, isolation

Large scale production of cheap, thinned modules

**Inner Trackers - Pixels**

Predominantly p-type

layers 2 - 4 : 5 x $10^{15}$ - 1.5 x $10^{15}$ $n_{eq}$

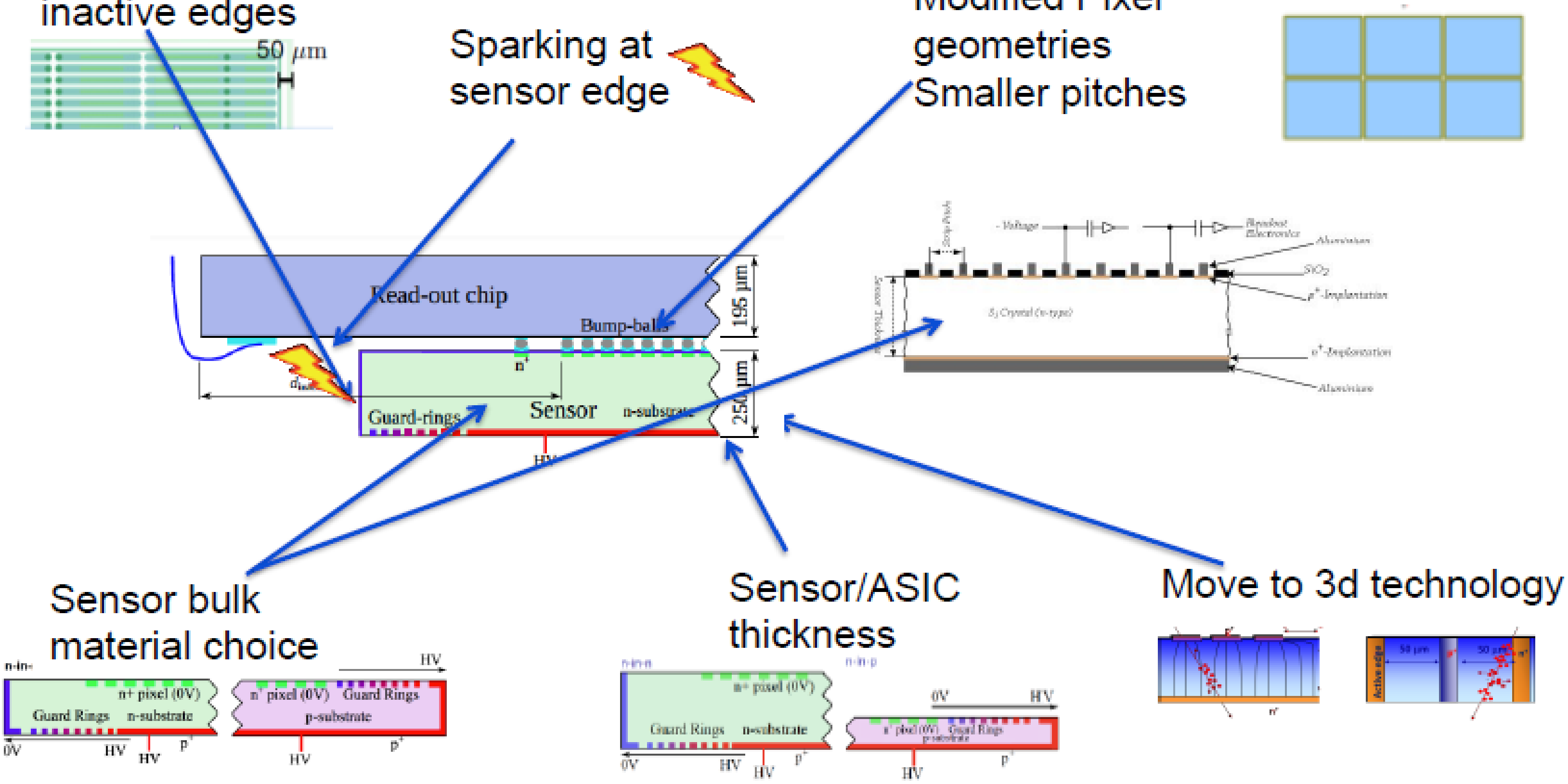
layer 1 : up to 2 x $10^{16}$: planar/3D/Diamond?

Explore process limits for fine pitch sensors

Sparking, Interconnection issue

Large scale production of cheap, thinned modules

# Current planar pixel detectors rad hard to ~ 10^15
# What are the HL-LHC baseline solutions?
# What are the challenges?



ROC tiling
on large sensor

Decreasing
inactive edges

Sparking at
sensor edge

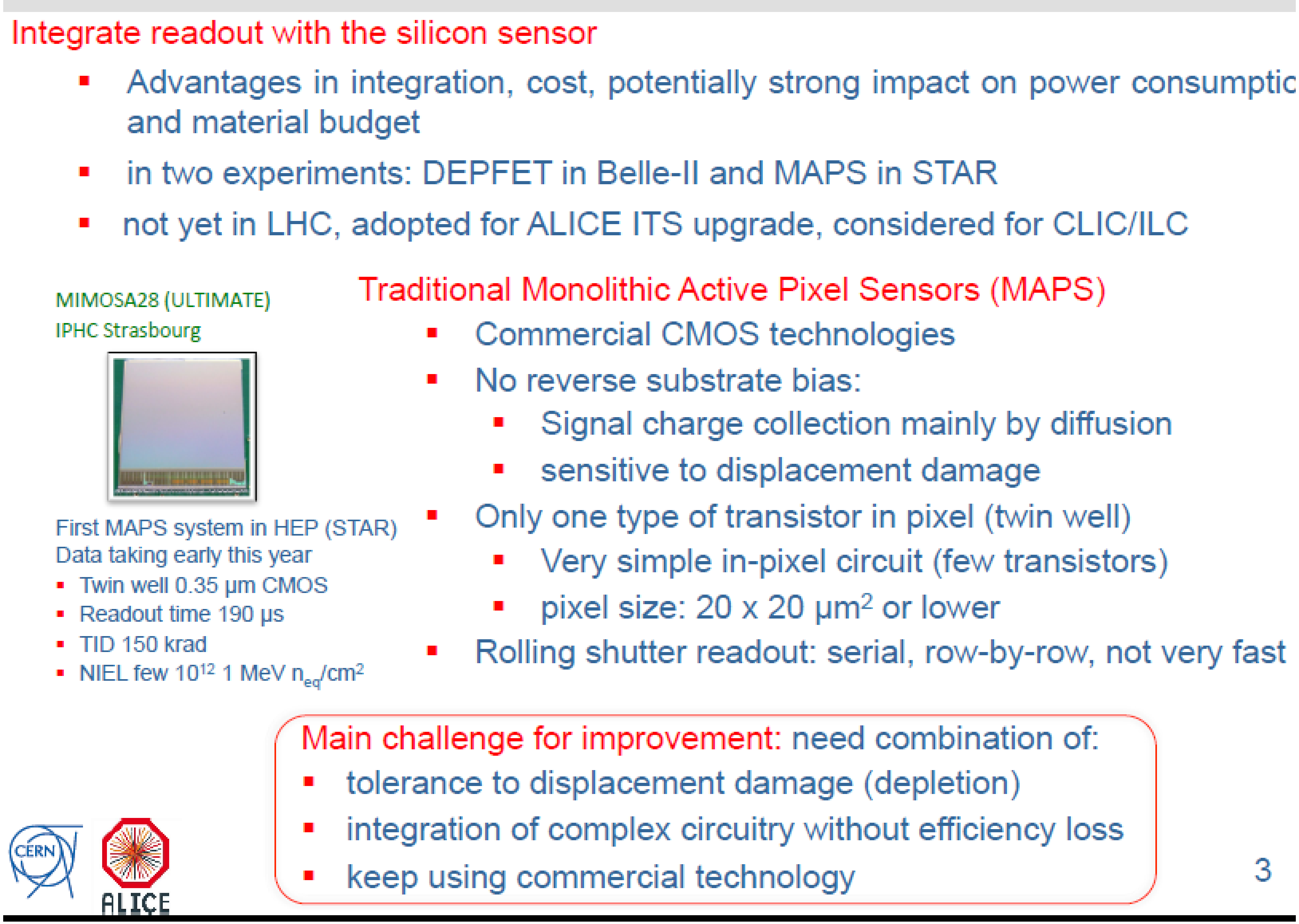
Modified Pixel
geometries
Smaller pitches

Sensor bulk
material choice

Sensor/ASIC
thickness

Move to 3d technology

# Future trend example



Integrate readout with the silicon sensor

- Advantages in integration, cost, potentially strong impact on power consumptic and material budget
- in two experiments: DEPFET in Belle-II and MAPS in STAR
- not yet in LHC, adopted for ALICE ITS upgrade, considered for CLIC/ILC

MIMOSA28 (ULTIMATE)
IPHC Strasbourg

First MAPS system in HEP (STAR)
Data taking early this year

- Twin well 0.35 µm CMOS
- Readout time 190 µs
- TID 150 krad
- NIEL few $10^{12}$ 1 MeV $n_{eq}/cm^2$

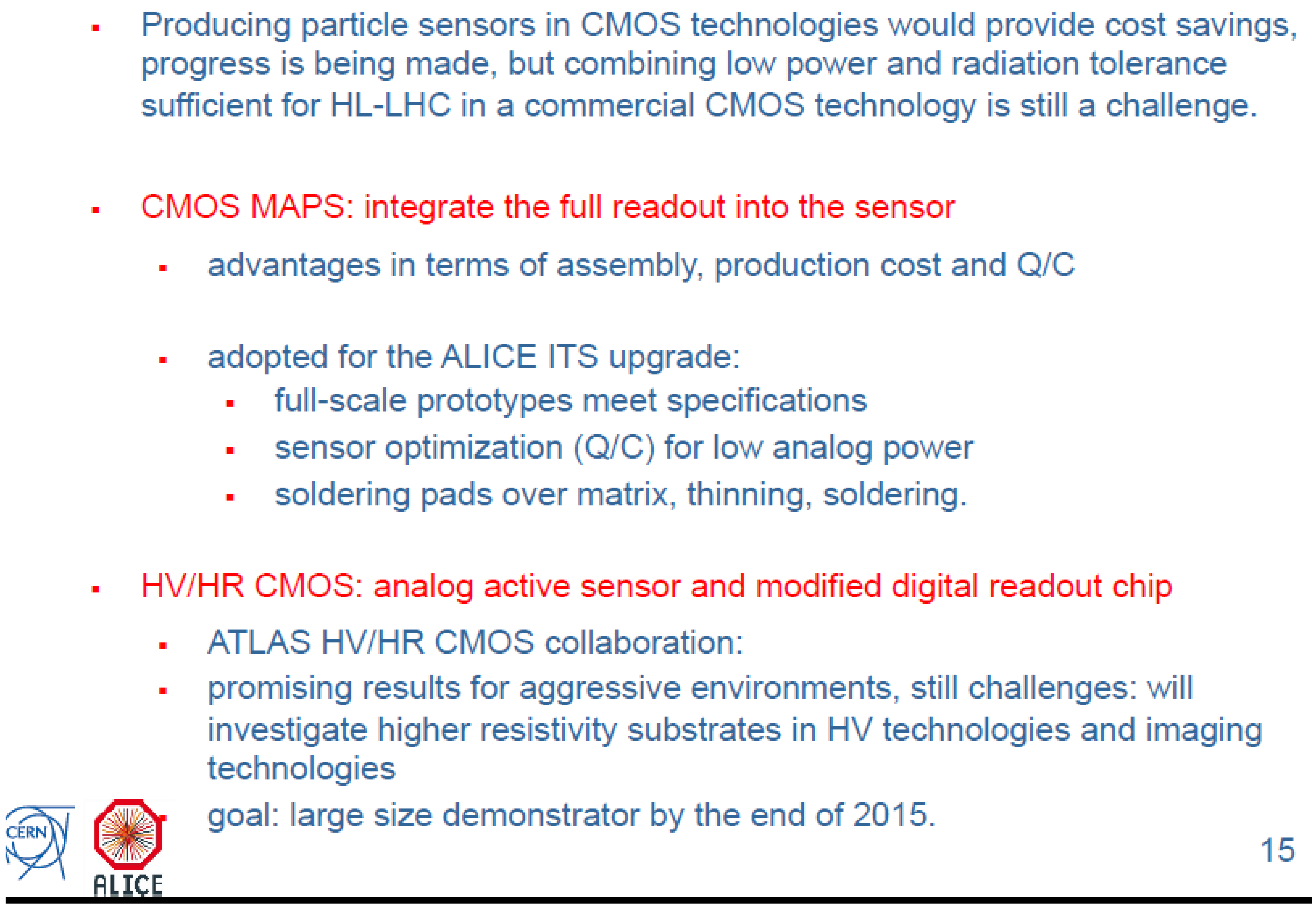
Traditional Monolithic Active Pixel Sensors (MAPS)

- Commercial CMOS technologies
- No reverse substrate bias:
  - Signal charge collection mainly by diffusion
  - sensitive to displacement damage
- Only one type of transistor in pixel (twin well)
  - Very simple in-pixel circuit (few transistors)
  - pixel size: 20 x 20 $\mu m^2$ or lower
- Rolling shutter readout: serial, row-by-row, not very fast

Main challenge for improvement: need combination of:

- tolerance to displacement damage (depletion)
- integration of complex circuitry without efficiency loss
- keep using commercial technology

From talk at ECFA 2014 meeting by W Snoeys



- Producing particle sensors in CMOS technologies would provide cost savings, progress is being made, but combining low power and radiation tolerance sufficient for HL-LHC in a commercial CMOS technology is still a challenge.
- CMOS MAPS: integrate the full readout into the sensor
  - advantages in terms of assembly, production cost and Q/C
  - adopted for the ALICE ITS upgrade:
    - full-scale prototypes meet specifications
    - sensor optimization (Q/C) for low analog power
    - soldering pads over matrix, thinning, soldering.
- HV/HR CMOS: analog active sensor and modified digital readout chip
  - ATLAS HV/HR CMOS collaboration:
  - promising results for aggressive environments, still challenges: will investigate higher resistivity substrates in HV technologies and imaging technologies
  - goal: large size demonstrator by the end of 2015.

From talk at ECFA 2014 meeting by W Snoeys